Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) ~~Processor~~ A processor for encrypting ~~and/or~~and decrypting data comprising:~~,~~

~~wherein~~ a control device is connected to at least one encryption/decryption means via at least one communication means, wherein, the control device comprises a memory and at least one external key input that receives an initial key from a source other than the key generation means, and

~~the control device is connected to~~ at least one ~~rounding~~ground key generation means connected to the control device via at least one further communication means, wherein the round key generation means receives a data word from the control device for calculating at least one round key and transfers the at least one round key to the memory of the storage device;

~~the control device has at least one external key input;~~

wherein the at least one encryption/decryption means ~~has~~ comprises at least one external data input for receiving the data, an input for receiving the at least one round key from the memory of the control device, ~~and~~ and at least one external data output for outputting data processed with the at least one round key, and

wherein the at least one encryption/decryption means and the at least one ~~rounding~~ground key generation means ~~are decoupled from one another~~communicate solely via the control device.

2. (Currently Amended) ~~A~~The processor ~~as claimed in~~of claim 1, ~~characterized~~ wherein ~~in that~~ the at least one communication means comprises at least one request line, at least one release line and at least one data line and/~~or~~ the at least one further communication means comprises at least one further request line, at least one further release line and at least one further data line.

3. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, characterized in that the at least one request line, the at least one release line and the at least one data line and/~~or~~ the at least one further request line, the at least one further release line and the at least one further data line at least partially use the same ~~line physics~~physical path.

4. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, ~~characterized in that the control device comprises at least one storage means in which at least one rounding key generated by~~ wherein the at least one ~~rounding~~round key ~~generation means can be~~is temporarily stored.

5. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of ~~claim 4~~claim 1, ~~characterized in that at least~~wherein the at least one round key from the memory of the control device is accessed using a ~~one~~ rotating pointer. ~~is provided for access to the at least one storage means.~~

6. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, ~~characterized in that~~wherein the ~~at least one handshake protocol is provided for~~ communication ~~of~~ between the control device ~~with~~ and the at least one encryption/decryption means and between the control device and ~~/or with~~ the at least one ~~rounding~~round key generation means is accomplished using at least one handshake protocol.

7. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, ~~characterized in that~~wherein the operation of ~~the modes of operation of~~ the control device, of the at least one encryption/decryption means and of the at least one ~~rounding~~round key generation means are asynchronous with respect to one another.

8. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, ~~characterized~~ wherein the round key generation means is adapted to perform a dummy operation. ~~in that at least one dummy calculation and/or at least part of at least one previous rounding key calculation can be carried out by means of the at least one rounding key generation means during at least one inactive phase.~~

9. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, ~~, characterized in that~~wherein ~~the~~ a time between ~~calculation~~ the calculating of the at least one round key by the round key generation means and the processing of the data using ~~and use of~~ the at least one ~~rounding~~round key is variable.

10. (Currently Amended) ~~A~~ The processor ~~as claimed in~~of claim 1, ~~characterized in that said~~wherein the processor ~~is embodied so as to be an~~is an AES coprocessor.

11. (Currently Amended) A method of encrypting and/or decrypting data using a processor ~~as claimed in claim 1,~~ comprising: ~~wherein~~

a) at least one initial key is read into a control device, wherein the at least one initial key is obtained from a source other than a round key generation means,

b) external data are read into at least one encryption/decryption means,

c) at least one data word needed to calculate at least one ~~rounding~~ground key is read from at least one storage means of the control device and transferred to at least one ~~rounding~~ground key generation means,

d) at least one ~~rounding~~ground key is calculated recursively on the basis of the at least one data word by means of the at least one ~~rounding~~ground key generation means, transferred to the control device and stored in the at least one storage means,

e) the at least one ~~rounding~~ground key is transferred from the at least one storage means to the at least one encryption/decryption means,

f) the external data are ~~encrypted or decrypted~~processed by means of the at least one encryption/decryption means using the at least one ~~rounding~~ground key and the ~~encrypted or decrypted~~processed data are made available at at least one external data output, and

g) steps b) to f) are repeated as often as necessary to encrypt or decrypt a set of external data.

12. (Currently Amended) ~~A~~The method ~~as claimed in~~ of claim 11, ~~characterized in that~~wherein the communication between ~~of~~ the control device with the at least one encryption/decryption means ~~and/or~~and between the control device and the at least one ~~rounding~~ground key generation means ~~takes place by means of~~is accomplished using at least one handshake protocol.

13. (Currently Amended) ~~A~~The method ~~as claimed in~~ of claim 11, wherein the operation of the control device, of the at least one encryption/decryption means and of the at least one round key generation means are asynchronous with respect to one another~~characterized in that the communication of the control device with the at least one encryption/decryption means and the at least one rounding key generation means takes place asynchronously~~.

14. (Currently Amended) ~~A~~The method ~~as claimed in~~ of claim 11, wherein the at least one round key from the memory of the control device is accessed using a ~~characterized in that access to the at least one storage means takes place by means of at least one~~ rotating pointer.

15. (Currently Amended) ~~A~~The method ~~as claimed in~~ of claim 11 further comprising performing a dummy operation using the round key generation means~~, characterized in that at least one dummy calculation and/or at least part of at least one previous rounding key calculation is carried out by means of the at least one rounding key generation means during at least one inactive phase~~.

16. (Currently Amended) ~~A~~The method ~~as claimed in~~ of claim 11, ~~characterized in that the~~ wherein a time between the calculating of the at least one round key by the round key generation means and the processing of the data using the at least one round key~~calculation and use of the at least one rounding key~~ is variable.

17. (Currently Amended) ~~A~~The method of claim 11, ~~as claimed in claim 10, characterized in that it is embodied as a method of AES calculation using an~~wherein the processor is an AES coprocessor ~~as claimed in claim 10~~.